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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,977	12/05/2001	Hiroyoshi Tanimoto	216648US2	1347

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EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,977	TANIMOTO ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-22* is/are pending in the application.

4a) Of the above claim(s) *17-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the filing of the amendment on 26 August 2003. Claims 1-3 and 5-22 are pending; claim 4 has been cancelled; claims 17-22 have been withdrawn from consideration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (5,510,630) in view of Zeng et al. (6,242,784).

Referring to claims 1 and 11, Agarwal et al. disclose a method of manufacturing a semiconductor device where a semiconductor element is formed in a semiconductor active region and calculating the generation rate of electron hole and a time integral of physical quantities. Agarwal et al. further disclose manufacturing a semiconductor device on the basis of the results (col. 3, lines 62 thru col. 4, line 4). Agarwal et al. do not disclose calculating the generation rate of electron hole pairs caused by impact ionization.

Zeng et al. disclose a method of manufacturing a semiconductor device where a semiconductor element is formed in a semiconductor active region, calculating the generation rate of electron hole pairs caused by impact ionization and evaluating time-

dependent variations of electrical characteristics of the semiconductor element (col. 2, lines 52-60).

Since Agarwal et al. and Zeng et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device, the purpose disclosed by Zeng et al. would have been recognized in the pertinent art of Agarwal et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Agarwal et al. by calculating the generation rate of electron hole pairs caused by impact ionization as taught by Zeng et al. to provide an efficient and reliable semiconductor device (col. 2, lines 52-54).

Referring to claims 2 and 5, Agarwal et al. disclose a method of manufacturing a semiconductor device where an insulated gate field effect transistor (14) is formed in the semiconductor active region on an insulated layer (37) of a substrate (16), in an electrically floating state (36). Agarwal et al. further disclose the insulated gate field effect transistor (14) formed in the semiconductor active region without any well electrode or body electrode (Fig. 3H, 4; col. 5, lines 12-56; col. 6, lines 17-60).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. in view of Zeng et al. as applied to claims 1, 2, 5 and 11 above, and further in view of Yamazaki et al. (6,184,556).

Agarwal et al. disclose a method of manufacturing a semiconductor device where an insulated gate field effect transistor (14) is formed in the semiconductor active region on an insulated layer (37) of a substrate (16), in an electrically floating state (36). Agarwal et al. further disclose the insulated gate field effect transistor (14) formed in the

semiconductor active region without any well electrode or body electrode (Fig. 3H, 4; col. 5, lines 12-56; col. 6, lines 17-60). Agarwal et al. do not disclose the substrate as sapphire.

Yamazaki et al. disclose a method of manufacturing a semiconductor device where a semiconductor device is formed on a sapphire substrate (col. 15, lines 46-51).

Since Agarwal et al. and Yamazaki et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device, the purpose disclosed by Yamazaki et al. would have been recognized in the pertinent art of Agarwal et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Agarwal et al. by having a sapphire substrate as taught by Yamazaki et al. to increase the selectivity between semiconductor layers (col. 15, lines 39-42).

Claims 6-10 and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. in view of Zeng et al. as applied to claims 1, 2, 5 and 11 above, and further in view of *Hot-Electron-Induced MOSFET Degradation-Model, Monitor and Improvement* Hu et al.

Agarwal et al. disclose a method of manufacturing a semiconductor device where a semiconductor element is formed in a semiconductor active region and calculating the generation rate of electron hole and a time integral of physical quantities. Agarwal et al. further disclose manufacturing a semiconductor device on the basis of the results (col. 3, lines 62 thru col. 4, line 4). Agarwal et al. also disclose a method of manufacturing a semiconductor device where an insulated gate field effect transistor (14) is formed in the

semiconductor active region on an insulated layer (37) of a substrate (16), in an electrically floating state. Agarwal et al. disclose the insulated gate field effect transistor (14) formed in the semiconductor active region without any well electrode or body electrode (Fig. 3H, 4; col. 5, lines 12-56; col. 6, lines 17-60). Agarwal et al. do not disclose evaluating time-dependent variations based on a threshold voltage, a driving current or creating data concerning the between stresses and variations of threshold voltage.

Hu et al. disclose a method of manufacturing a semiconductor device where time-dependent variations of electrically characteristics are evaluated based on the generation rate of electron hole pairs caused by impact ionization (pg. 375). Hu et al. disclose evaluating time-dependent variations of electrical characteristics of a semiconductor element on the basis of variations of a threshold voltage, ΔV_{th}, derived using the following equation:

$$\Delta V_{th} = A\ (I_{subQ}/Id)^{\alpha}\ Id^{\beta}$$

where I_{subQ} denotes a pseudo current of a semiconductor active region, Id denotes a drain current and A, α and β denote model parameters. Hu et al. disclose creating data about stresses and variations of the threshold voltage (pg. 377, 378). Hu et al. further disclose evaluating time-dependent variations of a driving current of a semiconductor device (pg, 378, 379). Hu et al. further disclose creating a physical model of the electron holes on the basis of the data and evaluations (pg. 380).

Since Agarwal et al. and Hu et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device, the purpose disclosed by Hu et al.

would have been recognized in the pertinent art of Agarwal et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Agarwal et al. by evaluating time-dependent variations based on a threshold voltage, a driving current or creating data concerning the between stresses and variations of threshold voltage as taught by Hu et al. to calculate and improve device life (pg. 383, 384).

Response to Arguments

Applicant's arguments filed 5 December 2001 have been fully considered but they are not persuasive. As stated above, Agarwal et al. in view Zeng et al. disclose the method of manufacturing a semiconductor device as described in claims 1 and 11.

In response to the applicant's arguments, the applicant argues the prior art does not teach the semiconductor active region being in a floating state. However, Agarwal et al. does disclose a method of manufacturing a semiconductor device where an insulated gate field effect transistor is formed in the semiconductor active region on an insulated layer of a substrate, in an electrically floating state (col. 7, lines 6-64).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (703) 605-4299. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PEP

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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